# 1P2J Digital Electronics 2

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## Questions

### 1. Multiplexers

(a). Figure 1 shows a multiplexer with enable. Write out its truth table.

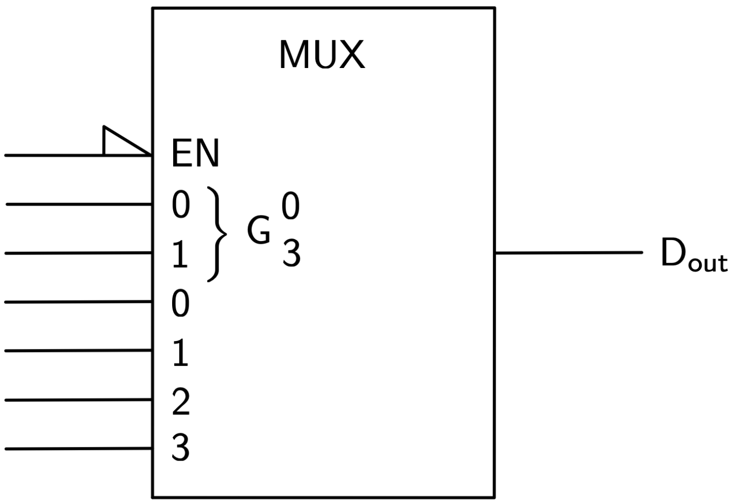


Figure 1

(b). Explain the meaning and consequences of the term "Fan Out".

(c). What is a tri-state output? Explain how such outputs enable a designer to connect together circuits using buses rather than complex logic circuits.

### 2. ROMs

(a). For the applications listed below select either a ROM, a PLA or an erasable/programmable ROM (EPROM) as a suitable component for the data storage and explain your reasons.

(i) Software code for a simple line following robot

(ii) Converting BCD code to drive a seven-segment display

(iii) A computer BIOS program

(iv) Software required to operate a scientific calculator.

(b). A ROM consists of an address decoder and an output matrix. Explain why the ROM decodes its address using more than one layer of gates.

## 3. PLAs

(a). A PLA has a programmable array of multi-input AND gates connected to its inputs and a programmable array of multi-input OR gates connected to its outputs. Explain how this differs from a ROM.

(b). Let $C_n$ represent the Carry-out from bit position $n$ during binary addition, $C_{n-1}$ thus being the Carry-In to position $n$ and the carry out from position $n-1$. For the sum $S = A + B$ demonstrate that

$$C_n = A_n.B_n + (A_n.\bar{B}_n + \bar{A}_n.B_n).C_{n-1}$$
$$S_n = \big(A_n.\bar{B}_n + \bar{A}_n.B_n\big).\bar{C}_{n-1} + (\bar{A}_n.\bar{B}_n + A_n.B_n).C_{n-1}$$

(c). Figure 2 (on the next page) shows a 5 input, 2 output PLA. A 2-bit Full Adder is to be designed with inputs $A_1$:$A_0$ and $B_1$:$B_0$ plus Carry-in, and outputs $S_1$:$S_0$ plus Carry-out. Indicate, using X's at the appropriate points on this diagram the connections to be made in the PLA to generate $S_0$ and Carry-out. Note that Carry-out here is equivalent to $C_1$.

## 4. State and Memory

(a). Figure 3 shows an OR gate with feedback. Initially the output is zero and $S$ is zero. A short duration pulse is applied to $S$. Draw a timing diagram of how the output changes in response.

Has this circuit recorded an event?

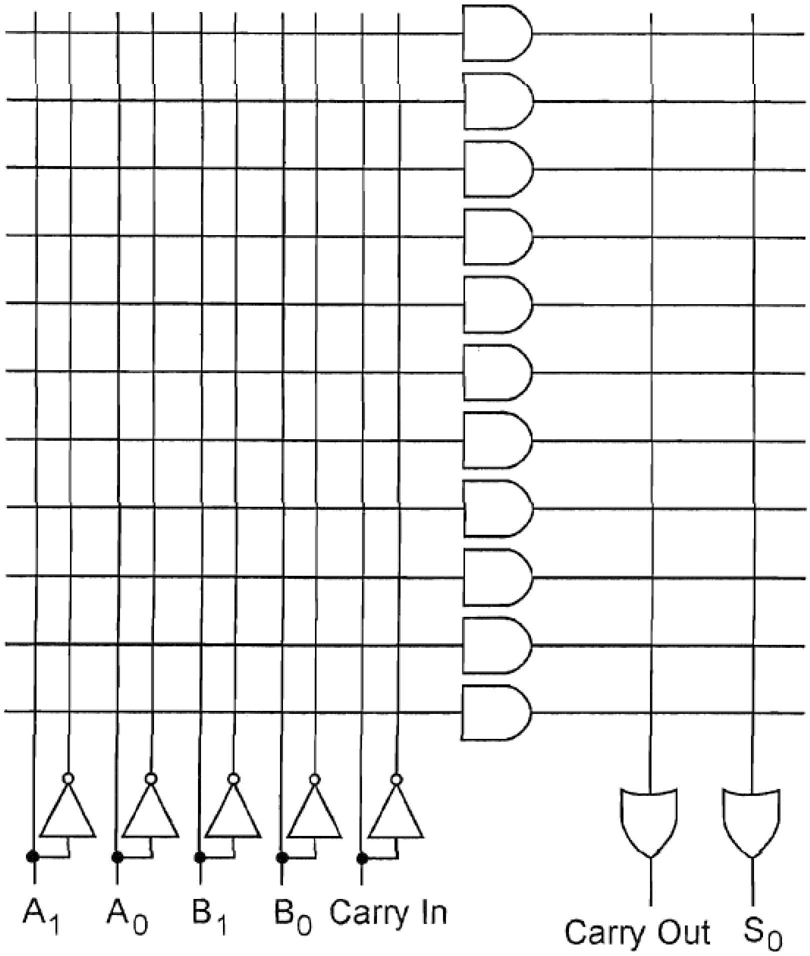


Figure 2

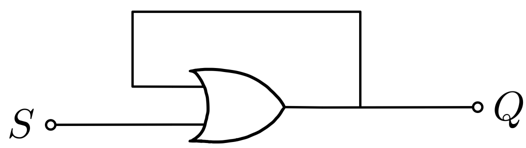


Figure 3

Does it have Memory?

Why is it not useful for storing data?

How should it be improved to make it more useful as a data storage device?

(b). What is the maximum number of states that may be represented by $n$ flip-flops?

## 5. Timing diagrams for memory elements

Suppose the input waveforms shown in Figure 4 are applied to the inputs of the following three types of memory elements.

(i) positive edge-triggered D-type flip-flop,

(ii) negative edge-triggered D-type flip-flop,

(iii) transparent D-latch with positive enable (clock).

Draw the waveforms for the $Q$ output in each of the three cases assuming that the initial value of the output is 0.

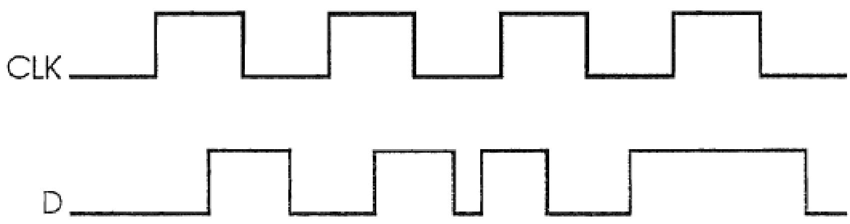


Figure 4

## 6. Asynchronous counters

(a). Design a modulo-5 asynchronous binary counter using positive edge triggered D-type flip flops with asynchronous reset. (Assume that the reset input is active-high and level sensitive. A modulo-5 counter counts from binary 000 to 100, and then back to 000).

(b). What determines the maximum speed at which the counter can run?

## 7. Synchronous Logic, Clocks, Flip-Flops

(a). Draw a circuit diagram for a simple 4-bit data register using D-type flip-flops.

(b). Figure 5 shows a simple sequencer built from positive edge triggered D-type flip flops. Initially all the flip-flop states are zero and then a start pulse is applied as indicated in the timing diagram. Draw a timing showing $Q_1$, $Q_2$, $Q_3$, CSL and CSP for 9 clock periods. Indicate on your diagram any edge dependencies between your signals.

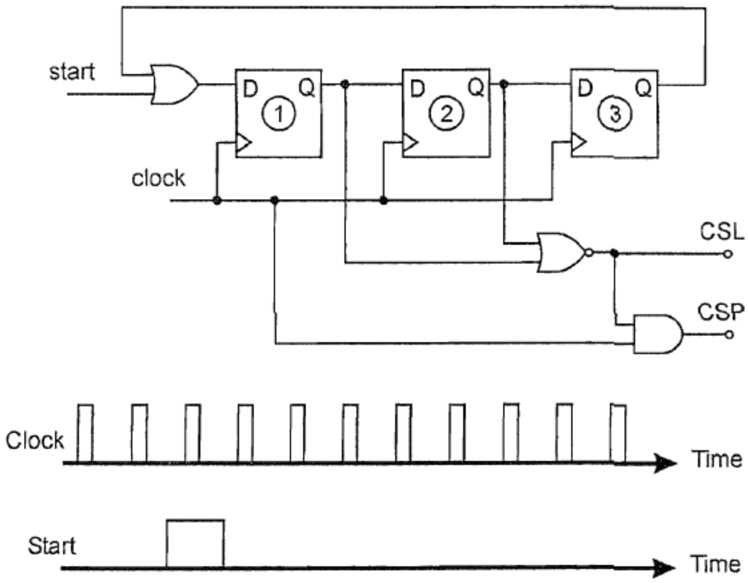


Figure 5

## 8. Synchronous counters

(a). Design a modulo-6 synchronous binary counter using D-type positive-edge triggered flip-flops.

(b). Your design will have two “don't care” states. What happens if the counter enters these states when being initialised, and how can the design be improved?

## 9. Simple state machines

A communications application requires two sequences of binary numbers to be generated. The two sequences are:

Sequence A: $0, 1, 2, 3$

Sequence B: $0, 3, 1, 2$

An external input called $C$ selects which sequence is to be generated: $C = 0$

should give sequence A and $C = 1$ should give sequence B.

(a). Design a digital circuit for realising the sequencer using two positive-edge triggered D-type flip-flops.

(b). Draw a typical circuit for an alternative ROM-based design.

(c). Tabulate the data entries recorded in the addressable space of the ROM.

## 10. Analogue to Digital Converter (ADC)

(a). Explain the purpose and function of each of the components of the Successive Approximation Converter shown in Figure 6.

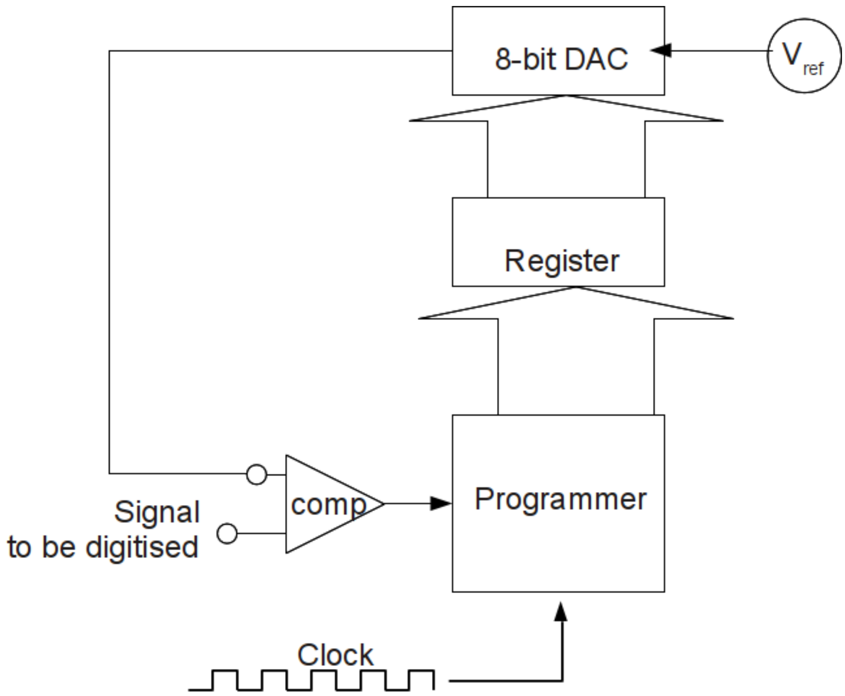


Figure 6: Successive Approximation ADC (block diagram)

(b). The Successive Approximation ADC in Figure 6 is to be used to digitise a time varying signal whose maximum frequency is 10 kHz and which is always positive. The ADC reference voltage is 1 V and each bit cycle of the converter requires 40 clock periods. If two 8-bit samples are to be acquired for each period of the signal what is the clock speed required to achieve this with 1 bit resolution?

(c). Explain why sample and hold is required in a successive approximation ADC if very high frequency signals are to be sampled.

(d). Why is sample and hold not required in a Flash ADC?

## 11. Digital to Analogue Converter (DAC)

(a). Figure 7 shows a 4-bit DAC implemented using an R-2R ladder. Explain how the circuit operates and indicate where the digital input bits are applied.

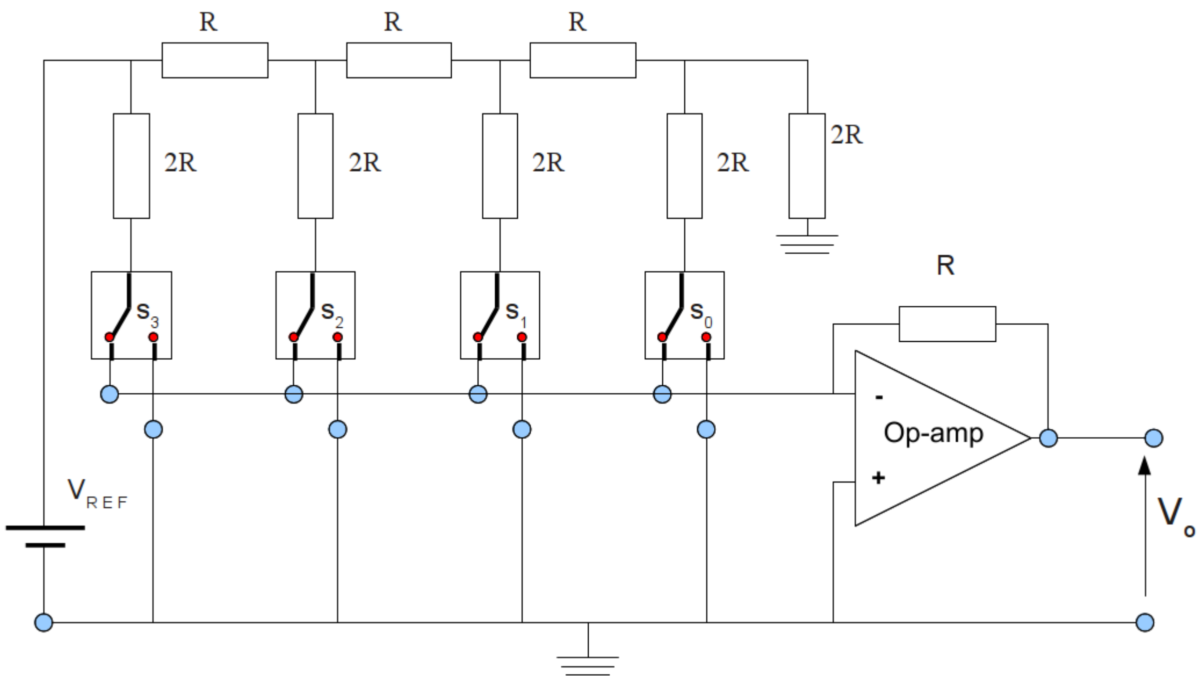


Figure 7: 4-bit DAC with R-2R ladder

(b). Show that the R-2R ladder results in currents at the switches that are rising as a power series.

(c). How can two DACs of this type be used to effectively multiply two 4-bit numbers together?

(d). Two DACs of the type shown are to be combined to create a single 8-bit DAC. Explain how this can be done and indicate what additional components are needed. Illustrate your answer with a diagram.

## Numerical Answers

10. (b). $5.15$ GHz